

ABSTRACT OF THE DISCLOSURE

An embodiment of a system for avoiding race conditions when using edge-triggered interrupts includes a processor that asserts an interrupt pending signal in response to the receipt of an edge-triggered interrupt. A power management device receives the interrupt pending signal. If the processor is in a low power state when it asserts the interrupt pending signal, then the power management device causes the processor to enter a high power state to allow the processor to service the pending interrupt.